EEE 3300 Electronics I (Summer 2018) PSPICE: Diode Applications

Diode Limiters, Rectifiers and Voltage Regulation (Due Tuesday, June 26, 2018)

Homework 2

Problem 1: Voltage Limiting

1.1. Simulate the following simple resistor-diode circuit (shown on the left in Figure 1):

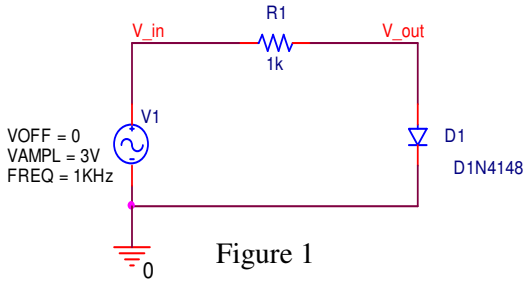
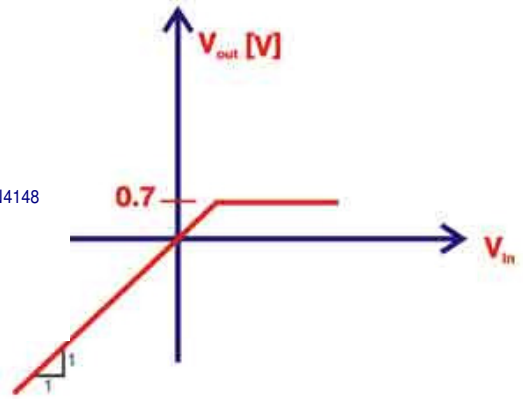


Figure 1



Let V(in) be a 1KHz VSIN with an amplitude of 3V. R1 is 1KΩ. Lowest node is ground.

(a) Set up PSPICE Transient and plot both V(in) and V(out) on the same scale. See that the upper part of V(out) is clipped at around 0.7V.

(b) Increase the amplitude of V(in) to 8V, and plot both V(in) and V(out) on the same scale and see that V(out) remains clipped at around 0.7V.

(c) Finally reduced the amplitude of V(in) to 100mV, and plot both V(in) and V(out) on the same scale and see that V(out)=V(in) (no clipping occurs).

Explanation: As long as V(in) is below the cut-in voltage of the diode (around 0.5V), the diode is OFF. Therefore V(out)=V(in). When the input voltage is such that the diode begins to conduct, V(out) becomes equal to a diode's forward voltage.

1.2. In Figure 1, replace V(in) with VDC, and do a DC Sweep, varying the input from -5V to +5V at increments of 0.1V. Observe V(out) as a function of V(in). You should see a curve similar to the diagram above (on the right – in this diagram the diode is assumed ideal). This is the input-output curve of the circuit. The circuit functions as a limiter. The limiter limits the output at 0.7V.

1.3. If we rotate the diode 180^0, diode will turn ON when V(in) falls below -0.5V. We thus obtain a limiter that lower limits at -0.7V. Repeat (1.1) and (1.2) for Figure 2:

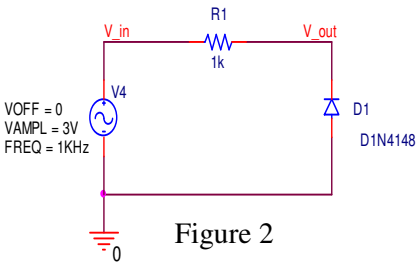
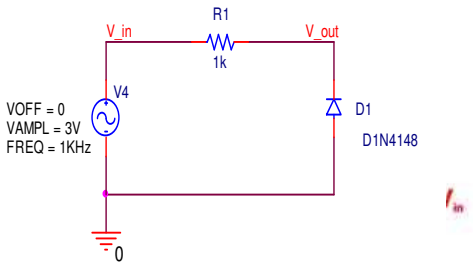


Figure 2



1.4. Now simulate the following two-diode circuit in Figure 3 for an upper and lower limits by |0.7| V:

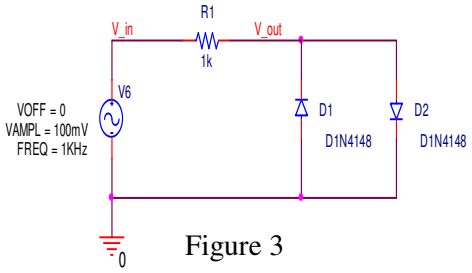
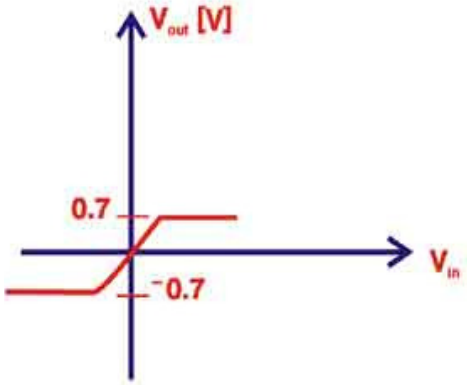


Figure 3



Simulate when V(in) is taken as VSIN with an amplitude of, say, 100mV, both diodes are OFF, and then V(out)=V(in). Next, simulate when V(in) has a larger amplitude, say 2V, both peaks of V(out) will come out clipped. Explain your simulation results for both cases.

1.5. We can set desired limiting levels by, conceptually, combining diodes and VDC sources, as shown below: Simulate the circuit in Figure 5 and explain your results.

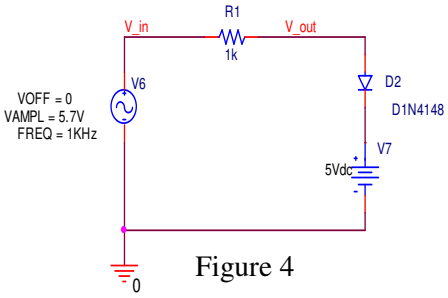
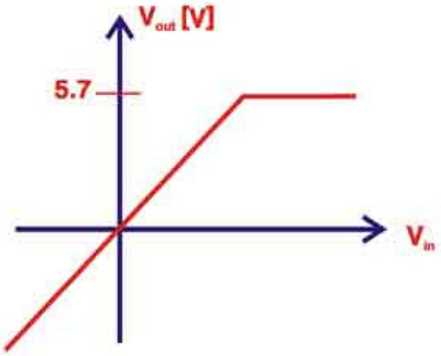


Figure 4



1.6. Practically though the VDC sources should be replaced by Zener diodes of appropriate size:

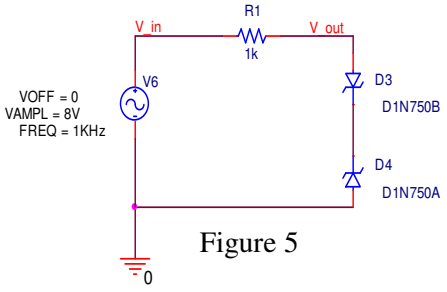
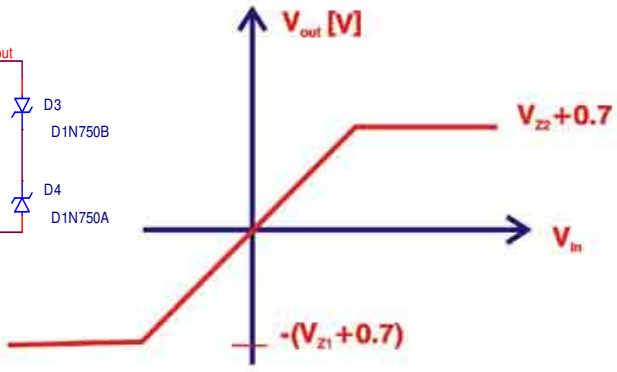


Figure 5



For instance, if we want a limiter we can use Zener diodes for Z_1 and Z_2. Use the 1N750 diode (default of 4.7V) for Z1 and Z2.The above values assume that the forward voltage of a Zener diode is 0.7V (as you can see, at limiting we always have one of the diodes in forward conduction mode). If the amplitude is smaller than the limiting levels, both diodes are OFF. Simulate the circuit in Figure 5 and explain how the circuit works.

Problem 2: Rectifier and Filter

2.1. See the Figure 2.1 below which is a simple half-wave rectifier and filter. The RC components perform "filtering" of the rectified signal. Using Transient, simulate and plot the output voltage of the half wave rectifier, for the following RC combinations:

a) $R_1 = 1k\Omega$, $C_1 = 1\mu F$
b) $R_1 = 10k\Omega$, $C_1 = 1\mu F$,
c) $R_1 = 10k\Omega$, $C_1 = 50\mu F$
d) $R_1 = 1k\Omega$, $C_1 = 200\mu F$.

Simulation time is 80ms. (Increase gradually the time constant RC). See how the ripples become smaller and smaller as RC increases. Measure and label the ripples peak-to-peak amplitudes for each RC combination using cursors.

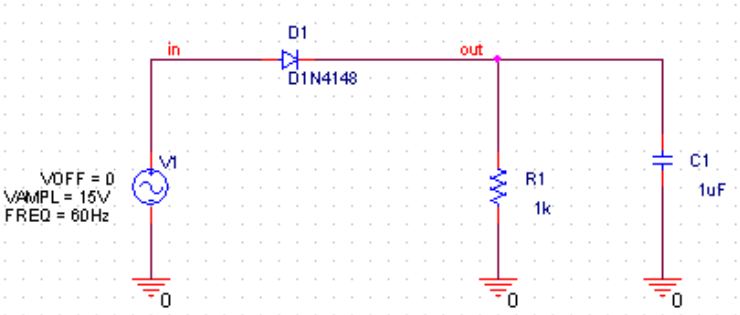


Figure 2.1. Simple Half Wave Rectifier

2.2. Referring to Figure 2.2, let us change the above VSIN source to an AC signal of amplitude 18V and frequency 150 Hz.

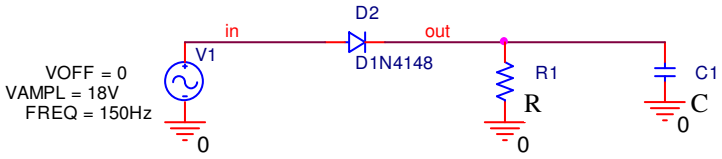


Figure 2.2. Simple Half Wave Rectifier

Design problem: Referring to Figure 2.2, this input signal needs to be converted to a rectified+filtered signal, with ripples amplitude of less than 1.2V. For that purpose, a half-wave rectifier and filter is used. How large should R and C be? Show all calculations and design formulas. (Don't use capacitor values larger than 200uF, or resistor values larger than 100kΩ). Also be aware that a too large value for R may cause the diode's current to be very small and it may degrade the diode's performance). For this part of the homework, you will need to refer to the RC design formula, given in Unit 13. Demonstrate that your design is successful, by measuring the ripples peak-to-peak with cursors. Use Transient with a run time of 5ms.

2.3. Design problem: Referring to Figure 2.3, this input signal needs to be converted to a rectified+filtered signal, with ripples amplitude of less than 1.2V. For that purpose, a full-wave rectifier consisting of a diode bridge and filter is used. How large should R and C be to meet the spec of ripples amplitude of less than 1.2V peak-to-peak? Show all calculations and design formulas. (Don't use capacitor values larger than 250uF, or resistor values larger than 100kΩ). Also be aware that a too large value for R may cause the diode's current to be very small and it may degrade the diode's performance). For this part of the homework, you will need to refer to the RC design formula, given in Unit 13. Demonstrate that your design is successful, by measuring the ripples peak-to-peak with cursors. Use Transient with a run time of 5ms.

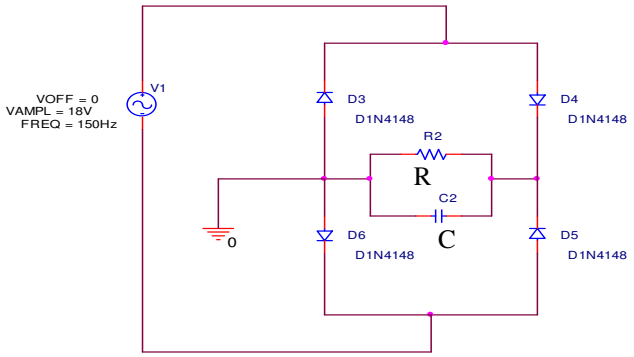


Figure 2.3. Full-Wave Diode Bridge Rectifier

Problem 3: Voltage Regulation (Read problem 3 completely first)

3.1. Design problem: Assume that a sinusoidal signal that has amplitude of 30V and a frequency of 440 Hz is the total secondary-side voltage of a center-tapped transformer as shown in Figure 3.1. Model that transformer by simply using two VSIN sources in series with ground in between; each VSIN source has amplitude of 15V. Using D1N4148 diodes, design a **full-wave rectifier** and filter, to obtain a (very crude) "DC voltage" of "15V minus one diode voltage" with ripples that are no bigger than 5% (ripples' peak-to-peak amplitude is considered with respect to the peak capacitor's voltage). Enter your initial PSPICE schematic and results to receive credit for this part of the homework. Formulas are required to show how the peak-to-peak ripple is related to your selected RC time constant. Use Transient with a run time of 10ms.

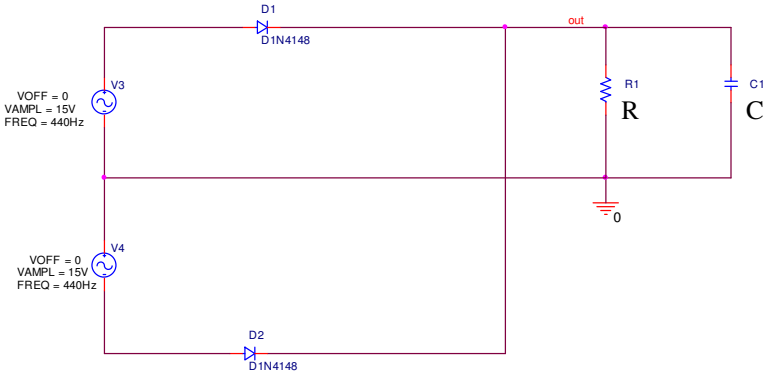


Figure 3.1. Full-Wave Diode Bridge Rectifier

3.2. Design and simulate a filtered full wave rectifier with a shunt regulator as shown in Figure 3.2. Need to redesign R and C based on some load current data and minimum Zener diode current spec. Assume that the filter's maximum voltage ripples are as in (3.1) above. The load current may vary between 0 and 15mA. You may represent it by a ISIN source hooked up in parallel to the Zener diode – make the current go from the Zener diode node to ground with IOFF of 7.5mA, IAMPL=7.5mA and FREQ=100Hz. [Precaution: As you hook up the ISIN source representing the load current make sure that this load takes away current from the Zener diode and does not add current to the Zener diode]. The design should assure that the Zener diode's current never falls below 7mA. Choose and explain your choice of R (following the theory of Unit 14) and, once you know what R is, revise C as necessary to keep the same filter ripples as before. Then demonstrate that the specs are met.

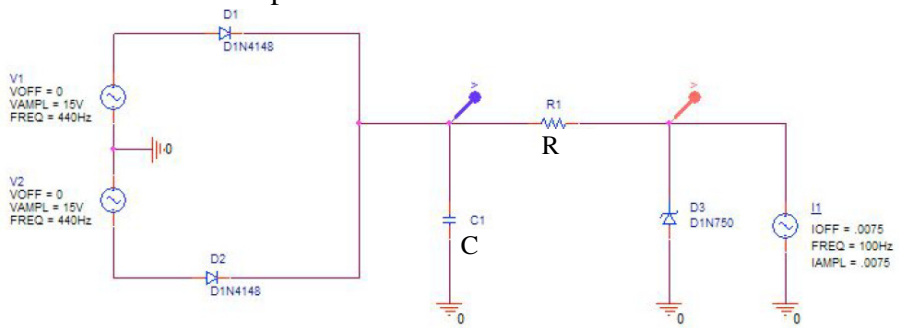


Figure 3.2. Full-Wave Diode Bridge Rectifier with Shunt Regulator

Hints to (3.1) and (3.2): For the full-wave rectifier:

1. The rectifier, filter and Zener voltage regulator should all be combined into a single circuit as shown in Figure 3.2. That means, for instance, that the Zener diode should be connected between the filter's resistor and ground - yes, use the same resistor for both the filter and the Zener driving! Because that resistor should allow sufficient current through the Zener diode, don't make it too large.

2. Calculate the effective zener voltage Vzo from the equation $V_{z0} = V_z - I_z R_z$ with Rz = 19Ω, Vz = 4.7V, Iz = 20mA
3. Calculate the value of the series resistor R (R1 in Figure 3.2) for the shunt regulator with the equation:

$$R \le \frac{V_{in}(min) - V_{z0} - I_z(min) R_z}{I_z(min) + I_L(max)}$$

   a. Vin(min) is the minimum input voltage, Vin(min) = Vp – 2*0.7 – Vr, Vp is the peak input voltage or 13.85V volts in this project, 0.7 volt is the voltage drop across one diode, Vr can be used as 258mV volts for an estimation.
   b. Vzo and Rz are obtained in step 2
   c. Iz(min) = 7mA is the minimum current needed for the zener diode to operate properly.
4. IL(max) = 15mA is the maximum load current. IL(min) = 0
5. Simulate your filtered full wave rectifier with a shunt regulator as shown in Figure 3.2.

Homework Solution Format: Each simulation solution must be typed and submitted on a hard copy printout only stapled at the upper left corner, neatly edited and should include the following items: Homework grade includes technical content and presentation (neatness and narration)!

1) Some calculations (in case of a design exercise) predicting approximately the expected outcome. Always explain your design considerations.
2) Printout of the circuit diagram – **print your name on each circuit diagram sheet**.
3) Output printouts – Be selective and use only the most relevant output. **Don't dump on the grader your entire collection of computer printouts**. In particular, never submit graphs that you cannot explain. **Print your name on every result sheet that you submit.**
4) Annotations to the results: PSPICE allows you to put comments and annotations on all output graphs and circuit schematics. It is highly recommended (for best readability of your work) to include notes and computations directly on the output graph pages themselves.
5) Brief conclusions – Did the circuit work as expected? If the results are far from your hand-calculation prediction, where is the difference coming from?

6) All Homework Assignments must be typed!

Homework is worth 5% of the total course grade. Maximum grade will be lowered if: a) Work is submitted past the deadline, and/or b) Suspected "Group Effort" – it's okay to work together in a team and consult each other; No "file sharing" with other groups or individuals!

Problems 1.1, 1.2, 1.3, 1.4, 1.5, and 1.6 above will initially be graded on a scale of 0-36. Problem 2 above will be initially being graded on a scale 0-24. Problem 3 above will initially be graded on a scale of 0-40.The total grade (maximum of 100 points).

Deadline for submission:

- **Upload a soft-copy of your Individual Homework 1 assignment to Canvas by the 1:00PM deadline on Tuesday, June 26, 2018 to turn in. Your name should be (typed) on each page of the assignment.**
- **File should be Microsoft WORD document only. A single Individual UPLOAD is allowed.**
- **To receive a graded copy of your homework 1 assignment, bring a hard-copy of your assignment to room FL-427 on, June 26, 2018 to turn in at Quiz 1.**
- **No emailed homework assignments accepted.**

  Late Homework assignment not accepted.